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AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0002] with the following amended paragraph:

[0002] This application is related to ~~the following~~ co-pending U.S. Patent Application Serial No. 10/730,703, filed on 12/09/2003, now U.S. Patent No. 6,965,254. The aforementioned application is commonly owned and has at least ~~, which is filed on the same day as this application, which has a common assignee and at least~~ one common inventor, and ~~which is hereinis~~ herein incorporated by reference in its entirety for all intents and purposes:

~~SERIAL NUMBER~~	~~DOCKET NUMBER~~	~~TITLE~~
~~----------~~	~~CNTR.2196~~	~~DYNAMIC LOGIC REGISTER~~

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0006] A dynamic logic return-to-zero (RTZ) latching mechanism according to an embodiment of the present invention includes a complementary pair of evaluation devices responsive to a clock signal, a dynamic evaluator, delayed inversion logic, and latching logic. The dynamic evaluator is coupled between the complementary pair of evaluation devices at a pre-charged node and evaluates a logic function based on at least one input data signal. The delayed inversion logic receives the clock signal and outputs an evaluation complete signal which is a delayed and inverted version of the clock signal. The latching logic asserts the logic state of an output node based on the state of the pre-charged node during an evaluation period between an operative edge of the clock signal and the next edge of the evaluation complete signal, and returns the output node to zero between evaluation periods. The latching logic includes an N-channel pass device having a gate receiving said evaluation complete signal and a drain and source coupled between said pre-charged node and a pull-up control node; a first P-channel pull-up device having a gate receiving said evaluation complete signal and a drain and source coupled between

a source voltage and said pull-up control node; a second P-channel pull-up device having a gate coupled to said pull-up control node and a drain and source coupled between said source voltage and said output node; and an N-channel pull-down device having a gate coupled to said pull-up control node and a drain and source coupled between said output node and ground.

[0007] The dynamic evaluator may range from a simple device to a complex logic circuit. The delayed inversion logic may be implemented in any suitable manner. In one exemplary embodiment, the delayed inversion logic is implemented as a series chain of inverters. The dynamic logic RTZ latching mechanism may include added logic and added complementary logic that collectively operates to prevent a selected state of the output node. A footless latching domino circuit or the like may be added to convert the RTZ output to a registered output signal.

[0008] A dynamic latch circuit according to an embodiment of the present invention includes a dynamic circuit, a delayed inverter, and a latching circuit. The dynamic circuit pre-charges at least one pre-charged node while the clock signal is low and evaluates a logic function for controlling the state of the pre-charged node when the clock signal goes high. The delayed inverter receives the clock signal and provides an inverted delayed clock signal. The latching circuit controls the state of an output node based on the state of the pre-charged node(s) during each evaluation period beginning when the clock signal goes high and ending when the inverted delayed clock signal next goes low. Otherwise, the latching circuit asserts the output node to a zero logic state. Again, a footless latching domino circuit or the like may be added to convert the RTZ output to a registered output signal. The latching circuit includes a pass device that couples a second node to said at least one pre-charged node when said inverted delayed clock signal is high; a first pull-up device that pulls said second node high while said inverted delayed clock signal is low; a second pull-up device that pulls said output node high when said second node is low; and a pull-down device that pulls said output node low when said second node is high.

[0009] The dynamic circuit may be implemented as multiple dynamic circuits, each receiving a corresponding input signal and each pre-charging a corresponding pre-

charged node. The latching circuit may be implemented as multiple latching circuits, each coupled to a corresponding dynamic circuit, each receiving a corresponding input signal, and each having an output that is wire-ORed coupled to the output node. The use of multiple dynamic and corresponding latching circuits enables implementation of many different logic functions that may vary from very simple to very complex. In one exemplary embodiment, an exclusive-OR logic function is implemented.

[0010] A dynamic logic RTZ latching method according to an embodiment of the present invention includes pre-setting a first node while a clock signal is in a first logic state, dynamically evaluating a logic function to control the logic state of the first node when the clock signal transitions to a second logic state, delaying and inverting the clock signal and providing a delayed inverted clock signal, latching a logic state of an output node based on the logic state of the first node determined during an evaluation period beginning when the clock signal transitions to the second logic state and ending with the next corresponding transition of the delayed inverted clock signal, and returning the logic state of the output node to a low logic state between evaluation periods.

[0011] The method may include adding a latching domino circuit to the output node to provide a registered output signal. The method may include passing a logic state of the first node to a pull-up control node while the delayed inverted clock signal is in a high logic state, pulling the output node to a high logic state if the pull-up control node is in a low logic state, and pulling the output node to a low logic state if the first node is in a high logic state. The method may include keeping the pull-up control node at a high logic state while the delayed inverted clock signal is at a low logic state and also while the clock signal is at a low logic state.